REMARKS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art. Claims 1, 4, 7, 12, 17, 21-26, 29, 30, 34-36, 39, 45, and 48 have been amended. Claims 2, 3, 5, 6, 15, 16, 27, 28, 31-33, 37, 38, and 49-51 have been cancelled. No claims have been added. No new matter has been introduced as a result of these amendments.

The Examiner objected to claim 31 as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicants have cancelled claim 31. Therefore, the Applicants respectfully request the Examiner to withdraw the objection.

The Examiner rejected claims 1-11, 21-29 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicants have accordingly amended claims 1 and 21 in a manner consistent with the Examiner's i nterpretation. Therefore, the Applicants respectfully submit that claims 1 and 21, along with their dependent claims, are now in condition for allowance, and request withdrawal of the rejections.

The Examiner rejected claim 21 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants have amended claim 21 so as not

include transmission media. Applicant respectfully requests withdrawal of the rejections under 35 U.S.C. § 101.

The Examiner rejected claims 1-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,816,961 of Rice et al. (hereinafter referred to as "Rice"). Applicant respectfully disagree because the reference fails to describe each and every element of the invention as claimed in claims 1-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53.

Rice describes a system that swaps bytes by selecting which field in a destination register receives which field from a source register (Rice, column 2, lines 45-51). A second source register, corresponding to a result field select value, defines how the swaps from the first source register to the destination are to occur (Rice, column 6, lines 38 to column 7, line 6). Therefore, the system of Rice requires three registers, as specified in an instruction with 3 operands, to perform the described byte swapping scheme (Rice, Figure 4, elements 412, 416, and 420; Figure 5, elements 504, 508, and 524). Furthermore, Rice specifically provides that the assembly sub-instruction for the swap would include 3 registers to carry out the swap operation without destroying/overwriting any register except the result register (Rice, column 7, lines 18-21). As a result, Rice only describes a system that operates on three registers where distinct registers are provided for source fields and a result field.

Rice further describes a source register that includes a plurality of operation fields (Rice, column 2, lines 1-10). The fields contain 5-bit codes that trigger the various operations (*See* Rice, column 8, Table II). Rice explicitly teaches that "five bits [are] devoted to the operation field" where a 5-bit sequence determines what operation is to be performed (Rice, column 7, lines 51-53).

With respect to claim 1, as amended, the Applicants claim:

A method comprising:
responsive to receiving a single packed shuffle instruction
designating, with 3 bits, a first register storing a first operand having a set of L data elements and designating, with 3 bits, a second register storing a second operand having a set of L control elements, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size, and wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit occupying the most significant bit of each control element, the second portion being a position selection field that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion, storing a resultant operand in said first register having L resultant data elements of the same size as the L data elements and the L control elements, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element, and is either,
the one of the L data elements designated by the position selection field of said control element if said control element's fl ush to zero bit is not set; or
a zero if said control element's fl ush to zero bit is set.

The Applicants respectfully submit that Rice fails to describe each and every feature as claimed in claim 1.

Rice only describes a system which utilizes three registers for swapping bytes of data. The three registers of Rice are explicitly illustrated in Figures 4 and 5, along with accompanying text. Although a value is written to the results register. Furthermore, the result field operation field values are comprised of 5-bit codes, as illustrated in Rice (column 8, Table I). Therefore, the reference fails to describe an each and every element as claimed by the Applicant in amended claim 1.

Hence, claim 1 is not anticipated by Rice for at least the reasons noted above. Furthermore, claims 2-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53 contain similar features and limitations to those discussed above with respect to claim 1. Thus, for similar reasons, claims 2-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53 are also not anticipated by Rice, for similar reasons to those advanced with respect to claim 1. Therefore, the Applicant respectfully requests withdrawal of the rejections of claim 1-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53 under 35 U.S.C. § 102, and submit that the claims are in condition for allowance.

The Examiner rejected claims 11, 20, and 22-27 under 35 U.S.C. § 103(a) as being unpatentable over Rice in view of Official Notice. However, as noted above, Rice fails to describe each and every feature as claimed by the Applicants

with respect to claims 1, 12, 21. Because the official notice merely covers operand types, the official notice also fails to describe or suggest the features deficient from Rice. Since neither Rice nor Official notice, describe or suggest the elements claimed in claims 11, 20, and 22-27, which depend from claims 1, 12, and 21, and include additional features and limitations, claims 11, 20, and 22-27 are also patentable over Rice in view of Examiner's Official Notice. Therefore, the Applicants respectfully request withdrawal of the rejections of claims 11, 20, and 22-27 under 35 U.S.C. § 103, and submit that the claims are in condition for allowance.

The Examiner rejected claims 6, 16-17, 28, 33-35, 38, and 50 under 35 U.S.C. § 103(a) as being unpatentable over Rice in view of U.S. Patent Application Publication 2002/0002666 of Dulong et al. (hereinafter "Dulong"). As discussed above, with respect to independent claims 1, 12, 21, 30, 36, and 48, from which claims 6, 16-17, 28, 33-35, 38, and 50 depend, Rice fails to describe or suggest each and every limitation claimed by the applicants in claims 1, 12, 21, 30, 36, and 48. Dulong describes a 4 register system where data from two or more source registers are transferred to a destination register based on the contents of a condition register (Dulong, Figure 2). Elements within the condition field merely select the value the two or more source registers to store in the result, thereby creating a combination of the source registers (Dulong, paragraph 0024). Because Dulong merely combines source registers, Dulong also

fails to describe or suggest the limitations discussed above with respect to claims 1, 12, 21, 30, 36, and 48. Therefore, Rice and Dulong, alone or in combination, fail to render claims 1, 12, 21, 30, 36, and 48, and thus dependent claims 6, 16-17, 28, 33-35, 38, and 50, obvious.

The Examiner rejected claims 39-47 under 35 U.S.C. § 103(a) as being unpatentable over Rice in view of U.S. Patent Application Publication 2005/0188182 of Hoyle et al. (hereinafter "Hoyle"). Similar to the discus sion above, with respect to independent claim 1, Rice similarly fails to describe or suggest each and every element of amended independent claims 39 and 45. Hoyle discusses a system where instructions perform byte intermingling from two source operands and store a result in a third result operand (Hoyle, Abstract). Because the various three-operand byte intermingling instructions merely perform predefined intermingling operations (*See* Hoyle, Table 9), Hoyle similarly fails to teach or suggest the limitations noted above. Therefore, for reasons similar to those discussed with respect to claim 1, Rice and Hoyle, alone or in combination fail to describe or suggest the limitations recited in claims 39 and 45, along with their respective dependent claims. The Applicants therefore respectfully request withdrawal of the rejections.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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